CLAIMS

Amend the claims as follows.

1. (Original) A dual port semiconductor memory cell, comprising:

a first CMOS inverter including a first NMOS transistor, a first PMOS transistor, an input port, and an output port;

a second CMOS inverter including a second NMOS transistor, a second PMOS transistor, an input port coupled to the output port of the first CMOS inverter and constitutes a first memory node together with the output port of the first CMOS inverter, and an output port coupled to the input port of the first CMOS inverter and constitutes a second memory node together with the input port of the first CMOS inverter;

a third NMOS transistor having a gate coupled to a wordline, a drain coupled to a bitline, and a source coupled to the first memory node;

a fourth NMOS transistor having a gate coupled to the wordline, a drain coupled to a complementary bitline, and a source coupled to the second memory node; and

a third PMOS transistor having a gate coupled to a scan address line, a source coupled to the second memory node, and a drain coupled to a scan data-out line.

2. (Previously presented) A dual port semiconductor memory cell ~~of claim 1~~, comprising:

a first CMOS inverter including a first NMOS transistor, a first PMOS transistor, an input port, and an output port;

a second CMOS inverter including a second NMOS transistor, a second PMOS transistor, an input port coupled to the output port of the first CMOS inverter and constitutes a first memory node together with the output port of the first CMOS inverter, and an output port coupled to the input port of the first CMOS inverter and constitutes a second memory node together with the input port of the first CMOS inverter;

a third NMOS transistor having a gate coupled to a wordline, a drain coupled to a bitline, and a source coupled to the first memory node;

a fourth NMOS transistor having a gate coupled to the wordline, a drain coupled to a complementary bitline, and a source coupled to the second memory node; and

a third PMOS transistor having a gate coupled to a scan address line, a source coupled to the second memory node, and a drain coupled to a scan data-out line;

where the memory cell is divided into first and second n-wells where P+ active regions are formed and first and second p-wells where N+ active regions are formed.

3. (Original) The dual port semiconductor memory cell of claim 2 where the first p-well, the second p-well, the first n-well, and the second n-well are arranged on the semiconductor substrate in an alternating manner.

4. (Original) The dual port semiconductor memory cell of claim 3 where the bitline and the complementary bit line and the scan data-out line are arranged in parallel with boundaries among the first and second p-wells and the first and second n-wells.

5. (Original) The dual port semiconductor memory cell of claim 4 where the wordline and the scan address line are arranged in perpendicular to the boundaries among the first and second p-wells and the first and second n-wells.

6. (Original) The dual port semiconductor memory cell of claim 3 comprising wiring layers, which have fixed voltage potentials and are arranged on the same layer as the bitline and complementary bitline.

7. (Original) The dual port semiconductor memory cell of claim 6 where the bitline, the complementary bitline, and the wiring layers are arranged in an alternating manner.

8. (Original) The dual port semiconductor memory cell of claim 7 where a wiring layer that is arranged between the bitline and the complementary bitline is a power supply line.

9. (Original) A dual port semiconductor memory device with a substrate including a plurality of memory cells, each memory cell comprising:

a first CMOS inverter including a first NMOS transistor, a first PMOS transistor, an input port, and an output port;

a second CMOS inverter including a second NMOS transistor, a second PMOS transistor, an input port coupled to the output port of the first CMOS inverter and constitutes a first memory node together with the output port of the first CMOS inverter, and an output

port coupled to the input port of the first CMOS inverter and constitutes a second memory node together with the input port of the first CMOS inverter;

a third NMOS transistor having a gate coupled to a wordline, a drain coupled to a bitline, and a source coupled to the first memory node;

a fourth NMOS transistor having a gate coupled to the wordline, a drain coupled to a complementary bitline, and a source coupled to the second memory node; and

a third PMOS transistor having a gate coupled to a scan address line, a source coupled to the second memory node, and a drain coupled to a scan data-out line;

where the plurality of memory cells are arranged in symmetry with respect to boundaries thereamong.

10. (Previously presented) A dual port semiconductor memory device with a substrate including a plurality of memory cells, each memory cell comprising:

a first CMOS inverter including a first NMOS transistor, a first PMOS transistor, an input port, and an output port;

a second CMOS inverter including a second NMOS transistor, a second PMOS transistor, an input port coupled to the output port of the first CMOS inverter and constitutes a first memory node together with the output port of the first CMOS inverter, and an output port coupled to the input port of the first CMOS inverter and constitutes a second memory node together with the input port of the first CMOS inverter;

a third NMOS transistor having a gate coupled to a wordline, a drain coupled to a bitline, and a source coupled to the first memory node;

a fourth NMOS transistor having a gate coupled to the wordline, a drain coupled to a complementary bitline, and a source coupled to the second memory node; and

a third PMOS transistor having a gate coupled to a scan address line, a source coupled to the second memory node, and a drain coupled to a scan data-out line;

where the plurality of memory cells are arranged in symmetry with respect to boundaries thereamong; and

where the memory cell is divided into first and second n-wells where P+ active regions are formed and first and second p-wells where N+ active regions are formed.

11. (Original) The dual port semiconductor memory device of claim 10 where the first p-well, the second p-well, the first n-well, and the second n-well are arranged on the semiconductor substrate in an alternating manner.

12. (Original) The dual port semiconductor memory device of claim 11 where the bitline and the complementary bit line and the scan data-out line are arranged in parallel with boundaries among the first and second p-wells and the first and second n-wells.

13. (Original) The dual port semiconductor memory device of claim 12 where the wordline and the scan address line are arranged in perpendicular to the boundaries among the first and second p-wells and the first and second n-wells.

14. (Original) The dual port semiconductor memory device of claim 11 comprising wiring layers, which have fixed voltage potentials and are arranged on the same layer as the bitline and complementary bitline.

15. (Original) The dual port semiconductor memory device of claim 14 where the bitline, the complementary bitline, and the wiring layers are arranged in an alternating manner.

16. (Original) The dual port semiconductor memory device of claim 15 where a wiring layer that is arranged between the bitline and the complementary bitline is a power supply line.

17. (Original) A dual port semiconductor memory device comprising:

a semiconductor substrate which is divided into first and second n-wells having P+ active regions and first and second p-wells having N+ active regions, the second p-well being located between the first and second n-wells and the first and second p-wells including a plurality of memory cells located at either side of the first n-well;

a wordline and a scan address line;

a pair of bitlines, comprised of a bitline and a complementary bitline, and a scan data-out line;

where each of the plurality of memory cells comprises:

a first CMOS inverter which includes a first NMOS transistor, a first PMOS transistor, an input port, and an output port;

a second CMOS inverter which includes a second NMOS transistor , a second PMOS transistor, an input port, coupled to the output port of the first CMOS inverter and constitutes a first memory node together with the output port of the first CMOS inverter, and

an output port, coupled to the input port of the first CMOS inverter and constitutes a second memory node together with the input port of the first CMOS inverter;

a third NMOS transistor having a gate coupled to the wordline, a drain coupled to the bitline, and a source coupled to the first memory node;

a fourth NMOS transistor having a gate coupled to the wordline, a drain coupled to the complementary bitline, and a source coupled to the second memory node; and

a third PMOS transistor having a gate coupled to the scan address line, a source coupled to the second memory node, and a drain coupled to the scan data-out line,

where the first and third NMOS transistors are formed in the N+ active regions of the first p-well, the second and fourth NMOS transistors are formed in the N+ active regions of the second p-well, the first and second PMOS transistors are formed in the P+ regions of the first n-well, and the third PMOS transistor is formed in the P+ active region of the second n-well.

18. (Original) The dual port semiconductor memory device of claim 17 where the plurality of memory cells are arranged in symmetry with respect to boundaries thereamong.

19. (Original) The dual port semiconductor memory device of claim 17 where the pair of bitlines and the scan data-out line are arranged in parallel with boundaries among the first and second p-wells and the first and second n-wells.

20. (Original) The dual port semiconductor memory device of claim 17 where the wordline and the scan address line are arranged in perpendicular to the boundaries among the first and second p-wells and the first and second n-wells.

21. (Original) The dual port semiconductor memory device of claim 17 comprising wiring layers, which have fixed voltage potentials and are arranged on the same layer as the pair of bitlines.

22. (Original) The dual port semiconductor memory device of claim 21 where the bitline, the complementary bitline, and the wiring layers are arranged in an alternating manner.

23. (Original) The dual port semiconductor memory device of claim 22 where a wiring layer arranged between the bitline and the complementary bitline is a power supply line.

24-33. (Cancelled)